

FORM PTO-1449  
(REV. 7-80)U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICEATTY. DOCKET NO.  
660073.587APPLICATION NO.  
08/798,227

## INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

DEC 15 1998

APPLICANT(S)  
Brent KeethFILING DATE  
February 11, 1997GROUP ART UNIT  
2306

## PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
DBR	AA	3,633,174	1/4/72	Griffin	<del>340</del>	<del>172.5</del>	
DBR	AB	4,077,016	2/28/78	Sanders et al.	<del>331</del>	<del>4</del>	
DBR	AC	4,096,402	6/20/78	Schroeder et al.	<del>307</del>	<del>362</del>	
DBR	AD	4,404,474	9/13/83	Dingwall	<del>307</del>	<del>260</del>	
DBR	AE	4,511,846	4/16/85	Nagy et al.	<del>328</del>	<del>164</del>	
DBR	AF	4,514,647	4/30/85	Shoji	<del>307</del>	<del>269</del>	
DBR	AG	4,600,895	7/15/86	Landsman	<del>331</del>	<del>1 A</del>	
DBR	AH	4,638,187	1/20/87	Boler et al.	<del>307</del>	<del>451</del>	
DBR	AI	4,687,951	8/18/87	McElroy	<del>307</del>	<del>269</del>	
DBR	AJ	4,773,085	9/20/88	Cordell	<del>375</del>	<del>120</del>	
DBR	AK	4,789,796	12/6/88	Foss	<del>307</del>	<del>443</del>	
DBR	AL	4,893,087	1/9/90	Davis	<del>328</del>	<del>14</del>	
DBR	AM	4,902,986	2/20/90	Lesmeister	<del>331</del>	<del>25</del>	
DBR	AN	4,958,088	9/18/90	Farah-Bakhsh et al.	<del>307</del>	<del>443</del>	
DBR	AO	4,984,204	1/8/91	Sato et al.	365	189.11	
DBR	AP	5,038,115	8/6/91	Myers et al.	<del>331</del>	<del>2</del>	
DBR	AQ	5,086,500	2/4/92	Greub	<del>395</del>	<del>550</del>	
DBR	AR	5,087,828	2/11/92	Sato et al.	<del>307</del>	<del>269</del>	
DBR	AS	5,122,690	6/16/92	Bianchi	<del>307</del>	<del>475</del>	
DBR	AT	5,128,560	7/7/92	Chern et al.	<del>307</del>	<del>475</del>	
DBR	AU	5,128,563	7/7/92	Hush et al.	<del>307</del>	<del>482</del>	
DBR	AV	5,134,311	7/28/92	Biber et al.	<del>307</del>	<del>270</del>	
DBR	AW	5,150,186	9/22/92	Pinney et al.	<del>357</del>	<del>42</del>	
DBR	AX	5,165,046	11/17/92	Hesson	<del>307</del>	<del>270</del>	
DBR	AY	5,179,298	1/12/93	Hirano et al.	<del>307</del>	<del>443</del>	

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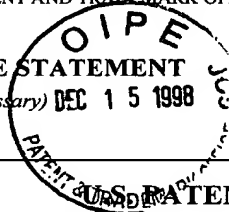
Group 2700

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DBR	BA	5,194,765	3/16/93	Dunlop et al.	307	<del>443</del>	
DBR	BB	5,220,208	6/15/93	Schenck	307	<del>443</del>	
DBR	BC	5,239,206	8/24/93	Yanai	307	<del>272.2</del>	
DBR	BD	5,243,703	9/7/93	Farmwald et al.	<del>395</del>	<del>325</del>	
DBR	BE	5,254,883	10/19/93	Horowitz et al.	307	<del>443</del>	
DBR	BF	5,256,989	10/26/93	Parker et al.	331	<del>1 A</del>	
DBR	BG	5,257,294	10/26/93	Pinto et al.	<del>375</del>	<del>120</del>	
DBR	BH	5,268,639	12/7/93	Gasbarro et al.	324	<del>158 R</del>	
DBR	BI	5,274,276	12/28/93	Casper et al.	307	<del>443</del>	
DBR	BJ	5,276,642	1/4/94	Lee	365	189.04	
DBR	BK	5,278,460	1/11/94	Casper	307	<del>296.5</del>	
DBR	BL	5,281,865	1/25/94	Yamashita et al.	307	<del>279</del>	
DBR	BM	5,283,631	2/1/94	Koerner et al.	307	<del>451</del>	
DBR	BN	5,295,164	3/15/94	Yamamura	375	<del>120</del>	
DBR	BO	5,311,481	5/10/94	Casper et al.	365	230.06	
DBR	BP	5,321,368	6/14/94	Hoelzle	<del>328</del>	<del>63</del>	
DBR	BQ	5,337,285	8/9/94	Ware et al.	365	227	
DBR	BR	5,347,177	9/13/94	Lipp	307	<del>443</del>	
DBR	BS	5,347,179	9/13/94	Casper et al.	307	<del>451</del>	
DBR	BT	5,355,391	10/11/94	Horowitz et al.	<del>375</del>	<del>36</del>	
DBR	BU	5,361,002	11/1/94	Casper	<del>327</del>	<del>530</del>	
DBR	BV	5,390,308	2/14/95	Ware et al.	<del>395</del>	<del>400</del>	
DBR	BW	5,400,283	3/21/95	Raad	365	203	
DBR	BX	5,408,640	4/18/95	MacIntyre et al.	<del>395</del>	<del>550</del>	
DBR	BY	5,416,436	5/16/95	Rainard	<del>327</del>	<del>270</del>	Received
DBR	BZ	5,420,544	5/30/95	Ishibashi	<del>331</del>	<del>11</del>	Nov 10 1998

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## U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
DBR	CA	5,428,311	6/27/95	McClure	327	276	
DBR	CB	5,430,676	7/4/95	Ware et al.	365	189.02	
DBR	CC	5,432,823	7/11/95	Gasbarro et al.	375	356	
DBR	CD	5,438,545	8/1/95	Sim	365	189.05	
DBR	CE	5,440,260	8/8/95	Hayashi et al.	327	278	
DBR	CF	5,440,514	8/8/95	Flannagan et al.	365	194	
DBR	CG	5,446,696	8/29/95	Ware et al.	365	222	
DBR	CH	5,448,193	9/5/95	Baumert et al.	327	156	
DBR	CI	5,451,898	9/19/95	Johnson	327	563	
DBR	CJ	5,457,407	10/10/95	Shu et al.	326	30	
DBR	CK	5,473,274	12/5/95	Reilly et al.	327	159	
DBR	CL	5,473,575	12/5/95	Farmwald et al.	365	230.06	
DBR	CM	5,473,639	12/5/95	Lee et al.	375	376	
DBR	CN	5,485,490	1/16/96	Leung et al.	375	371	
DBR	CO	5,488,321	1/30/96	Johnson	327	66	
DBR	CP	5,497,127	3/5/96	Sauer	331	17	
DBR	CQ	5,498,990	3/12/96	Leung et al.	327	323	
DBR	CR	5,506,814	4/9/96	Hush et al.	365	230.03	
DBR	CS	5,508,638	4/16/96	Cowles et al.	326	38	
DBR	CT	5,513,327	4/30/96	Farmwald et al.	395	309	Received
DBR	CU	5,539,345	7/23/96	Hawkins	327	150	Mar 10 1998
DBR	CV	5,552,727	9/3/96	Nakao	327	159	Group 2700
DBR	CW	5,568,077	10/22/96	Sato et al.	327	199	
DBR	CX	5,572,557	11/5/96	Aoki	375	376	
DBR	CY	5,574,698	11/12/96	Raad	365	230.06	
DBR	CZ	5,576,645	11/19/96	Farwell	327	94	

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David Ranson

March 30, 1999

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*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
DBR	DA	5,578,940	11/26/96	Dillon et al.	326	30	
DBR	DB	5,578,941	11/26/96	Sher et al.	326	34	
DBR	DC	5,579,326	11/26/96	McClure	371	61	
DBR	DD	5,581,197	12/3/96	Motley et al.	326	30	
DBR	DE	5,589,788	12/31/96	Goto	327	276	
DBR	DF	5,590,073	12/31/96	Arakawa et al.	365	185.08	
DBR	DG	5,594,690	1/14/97	Rothenberger et al.	365	189.01	
DBR	DH	5,614,855	3/25/97	Lee et al.	327	158	
DBR	DI	5,619,473	4/8/97	Hotta	365	238.5	
DBR	DJ	5,621,340	4/15/97	Lee et al.	327	65	
DBR	DK	5,621,690	4/15/97	Jungroth et al.	365	200	
DBR	DL	5,621,739	4/15/97	Sine et al.	371	22.1	
DBR	DM	5,627,780	5/6/97	Malhi	365	185.09	
DBR	DN	5,627,791	5/6/97	Wright et al.	365	222	
DBR	DO	5,631,872	5/20/97	Naritake et al.	365	227	
DBR	DP	5,636,163	6/3/97	Furutani et al.	365	189.04	
DBR	DQ	5,636,174	6/3/97	Schaefer	365	230.03	Received
DBR	DR	5,636,174	6/3/97	Rao	365	230.03	10 19
DBR	DS	5,638,335	6/10/97	Akiyama et al.	365	230.03	Group 270
DBR	DT	5,657,481	8/12/97	Farmwald et al.	395	551	
DBR	DU	5,668,763	9/16/97	Fujioka et al.	365	200	
DBR	DV	5,694,065	12/2/97	Hamasaki et al.	327	108	
DBR	DW	5,712,580	1/27/98	Baumgartner et al.	327	12	
DBR	DX	5,751,665	5/12/98	Tanoi	368	120	

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David Hanson

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## FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
DBR	EA	6-1237512	10/22/86	JP (Abstract Only)			X	
DBR	EB	0 295 515 A1	12/21/88	EP			X	
DBR	EC	2-112317	4/25/90	JP (+ Abstract)				X
DBR	ED	0 406 786 A1	1/9/91	EP			X	
DBR	EE	0 450 871 A2	10/9/91	EP			X	
DBR	EF	4-135311	8/5/92	JP (+ Abstract)				X
DBR	EG	5-136664	1/6/93	JP (+ Abstract)				X
DBR	EH	5-282868	10/29/93	JP (Abstract Only)			X	
DBR	EI	0 655 741 A2	5/31/95	EP			X	
DBR	EJ	0 655 834 A1	5/31/95	EP			X	
DBR	EK	WO 95/22200	8/17/95	PCT			X	
DBR	EL	WO 95/22206	8/17/95	PCT			X	
DBR	EM	0 680 049 A2	11/2/95	EP			X	
DBR	EN	0-7319577	12/8/95	JP (Abstract Only)			X	
DBR	EO	0 703 663 A1	3/27/96	EP			X	
DBR	EP	0 704 848 A2	4/3/96	EP			X	
DBR	EQ	0 704 975 A1	4/3/96	EP			X	
DBR	ER	WO 96/10866	4/11/96	PCT			X	
DBR	ES	0 767 538 A1	4/9/97	EP			X	
DBR	ET	WO 97/14289	4/24/97	PCT			X	
DBR	EU	WO 97/42557	11/13/97	PCT			X	

## OTHER PRIOR ART (Including Author, Title, Date, Pertinent Pages, Etc.)

DBR	EV	Alvarez, J. et al. "A Wide-Bandwidth Low Voltage PLL for PowerPC™ Microprocessors" IEEE IEICE Trans. Electron., Vol. E-78. No. 6, June 1995, pp. 631-639
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David Kansom

March 30, 1999

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<b>INFORMATION DISCLOSURE STATEMENT</b> <i>(Use several sheets if necessary)</i>				APPLICANT(S) Brent Keeth		GROUP ART UNIT 2306	
				FILING DATE February 11, 1997			
<b>OTHER PRIOR ART</b> <i>(Including Author, Title, Date, Pertinent Pages, Etc.)</i>							
DBR	FA		Anonymous, "Programmable Pulse Generator", IBM Technical Disclosure Bulletin, Vol. 17, No. 12, May 1975, pp. 3553-3554				
DBR	FB		Anonymous, "Pulse Combining Network", IBM Technical Disclosure Bulletin, Vol. 32, No. 12, May 1990, pp. 149-151				
DBR	FC		Anonymous, "Variable Delay Digital Circuit", IBM Technical Disclosure Bulletin, Vol. 35, No. 4A, September 1992, pp. 365-366				
DBR	FD		Arai, Y. et al., "A CMOS Four Channel x 1K Time Memory LSI with 1-ns/b Resolution", IEEE Journal of Solid-State Circuits, Vol. 27, No. 3, March, 1992, No.3, New York, US				
DBR	FE		Arai, Y. et al., "A Time Digitizer CMOS Gate-Array with a 250 ps Time Resolution", XP 000597207, IEEE Journal of Solid-State Circuits, Vol. 31, No.2, February 1996				
DBR	FF		Aviram, A. et al., "OBTAINING HIGH SPEED PRINTING ON THERMAL SENSITIVE SPECIAL PAPER WITH A RESISTIVE RIBBON PRINT HEAD", IBM Technical Disclosure Bulletin, Vol. 27, No. 5, October 1984, pp. 3059-3060				
DBR	FG		Bazes, M., "Two Novel Fully Complementary Self-Biased CMOS Differential Amplifiers", IEEE Journal of Solid-State Circuits, Vol. 26, No. 2, February 1991, pp. 165-168				
DBR	FH		Chapman, J. et al., "A Low-Cost High-Performance CMOS Timing Vernier for ATE", IEEE International Test Conference, Paper 21.2, 1995, pp. 459-468				
DBR	FI		Cho, J. "Digitally-Controlled PLL with Pulse Width Detection Mechanism for Error Correction", ISSCC 1997, Paper No. SA 20.3, pp. 334-335				
DBR	FJ		Christiansen, J., "An Integrated High Resolution CMOS Timing Generator Based on an Array of Delay Locked Loops", IEEE Journal of Solid-State Circuits, Vol. 31, No. 7, July 1996, pp. 952-957				
DBR	FK		Combes, M. et al., "A Portable Clock Multiplier Generator Using Digital CMOS Standard Cells", IEEE Journal of Solid-State Circuits, Vol. 31, No. 7, July 1996, pp. 958-965				
DBR	FL		Donnelly, K. et al., "A 660 MB/s Interface Megacell Portable Circuit in 0.3 $\mu$ m-0.7 $\mu$ m CMOS ASIC", IEEE Journal of Solid-State Circuits, Vol. 31, No. 12, December 1996, pp. 1995-2001				
DBR	FM		Goto, J. et al., "A PLL-Based Programmable Clock Generator with 50- to 350-MHz Oscillating Range for Video Signal Processors", IEICE Trans. Electron., Vol. E77-C, No. 12, December 1994, pp. 1951-1956				
DBR	FN		Hamamoto, T., "400-MHz Random Column Operating SDRAM Techniques with Self-Skew Compensation", IEEE Journal of Solid-State Circuits, Vol. 33, No. 5, May 1998, pp. 770-778				
DBR	FO		Ishibashi, A. et al., "High-Speed Clock Distribution Architecture Employing PLL for 0.6 $\mu$ m CMOS SOC" IEEE Custom Integrated Circuits Conference, 1992, pp. 27.6.1-27.6.4				
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				GROUP ART UNIT 2306			
<b>OTHER PRIOR ART</b> (Including Author, Title, Date, Pertinent Pages, Etc.)							
DBR	GA		Kim, B. et al., "A 30MHz High-Speed Analog/Digital PLL in 2 $\mu$ m CMOS", ISSCC, February 1990				
DBR	GB		Kikuchi, S. et al., "A GATE-ARRAY-BASED 666MHz VLSI TEST SYSTEM", IEEE International Test Conference, Paper 21.1, 1995, pp. 451-458				
DBR	GC		Ko, U. et al., "A 30-ps JITTER, 3.6- $\mu$ s LOCKING, 3.3-VOLT DIGITAL PLL FOR CMOS GATE ARRAYS", IEEE Custom Integrated Circuits Conference, 1993, pp. 23.3.1-23.3.4				
DBR	GD		Lee, T. et al., "A 2.5V Delay-Locked Loop for an 18Mb 500MB/s DRAM", IEEE International Solid-State Circuits Conference Digest of Technical Papers, Paper No. FA 18.6, 1994, pp. 300-301				
DBR	GE		Lesmeister, G., "A DENSELY INTEGRATED HIGH PERFORMANCE CMOS TESTER", International Test Conference, Paper 16.2, 1991, pp. 426-429				
DBR	GF		Ljuslin, C. et al., "An Integrated 16-channel CMOS Time to Digital Converter", IEEE Nuclear Science Symposium & Medical Imaging Conference Record, Vol. 1, 1993, pp. 625-629				
DBR	GG		Nakamura, M. et al., "A 156 Mbps CMOS Clock Recovery Circuit for Burst-mode Transmission", Symposium on VLSI Circuits Digest of Technical Papers, 1996, pp. 122-123				
DBR	GH		Nielson, E., "Inverting latches make simple VCO", EDN, June 19, 1997				
DBR	GI		Novof, I. et al., "Fully Integrated CMOS Phase-Locked Loop with 15 to 240 MHz Locking Range and $\pm 50$ ps Jitter", IEEE Journal of Solid-State Circuits, Vol. 30, No. 11, November 1995, pp. 1259-1266				
DBR	GJ		Santos, D. et al., "A CMOS Delay Locked Loop And Sub-Nanosecond Time-to-Digital Converter Chip", IEEE Nuclear Science Symposium and Medical Imaging Conference Record, Vol. 1, October 1995, pp. 289-291				
DBR	GK		Saeki, T. et al., "A 2.5-ns Clock Access, 250-MHz, 256-Mb SDRAM with Synchronous Mirror Delay", IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, November 1996, pp. 1656-1665				
DBR	GL		Shirotori, T. et al., "PLL-based, Impedance Controlled Output Buffer", 1991 Symposium on VLSI Circuits Digest of Technical Papers, pp. 49-50				
DBR	GM		Sidiropoulos, S. et al., "A 700-Mb/s/pin CMOS Signaling Interface Using Current Integrating Receivers", IEEE Journal of Solid-State Circuits, Vol. 32, No. 5, May 1997, pp. 681-690				
DBR	GN		Sidiropoulos, S. et al., "A CMOS 500 Mbps/pin synchronous point to point link interface", IEEE Symposium on VLSI Circuits Digest of Technical Papers, 1994, pp. 43-44				
DBR	GO		Sidiropoulos, S. et al., "A Semi-Digital DLL with Unlimited Phase Shift Capability and 0.08-400MHz Operating Range," in 1997 IEEE International Solid State Circuits Conference, February 8, 1997, pp.332-333				
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<b>OTHER PRIOR ART</b> (Including Author, Title, Date, Pertinent Pages, Etc.)							
DBR	HA		Soyuer, M. et al., "A Fully Monolithic 1.25GHz CMOS Frequency Synthesizer", IEEE Symposium on VLSI Circuits Digest of Technical Papers, 1994, pp. 127-128				
DBR	HB		Taguchi, M. et al., "A 40-ns 64-Mb DRAM with 64-b Parallel Data Bus Architecture", IEEE Journal of Solid-State Circuits, Vol. 26, November 1991, pp. 1493-1497				
DBR	HC		Tanoi, S. et al., "A 250-622 MHz Deskew and Jitter-Suppressed Clock Buffer Using a Frequency- and Delay-Locked Two-Loop Architecture", 1995 Symposium on VLSI Circuits Digest of Technical Papers, Vol. 11, No. 2, pp. 85-86				
DBR	HD		Tanoi, S. et. al., "A 250-622 MHz Deskew and Jitter-Suppressed Clock Buffer Using Two-Loop Architecture", IEEE IEICE Trans. Electron., Vol.E-79-C. No. 7, July 1996, pp.898-904				
DBR	HE		von Kaenel, V. et al., "A 320 MHz, 1.5 mW @ 1.35 V CMOS PLL for Microprocessor Clock Generation", IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, November 1996, pp. 1715-1722				
DBR	HF		Watson, R. et al., "Clock Buffer Chip with Absolute Delay Regulation Over Process and Environmental Variations", IEEE Custom Integrated Circuits Conference, 1992, pp. 25.2.1-25.2.5				
DBR	HG		Yoshimura, T. et al. "A 622-Mb/s Bit/Frame Synchronizer for High-Speed Backplane Data Communication", IEEE Journal of Solid-State Circuits, Vol. 31, No. 7, July 1996, pp. 1063-1066				
EXAMINER <i>David Hanson</i>				DATE CONSIDERED <i>March 30, 1998</i>			
* EXAMINER: Initial if reference considered, whether or not criteria is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).							

Form P7-27/V1/1/94 U:\vosiepl\IDS Adaptive Signal Timing

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